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MS APPEAL BRIEF - PATENTS
Docket No.: 0465-0883P
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jong KIM

Application No.: 10/029,198 — Confirmation No.: 5402

Filed: December 28, 2001 — Art Unit: 2629

For: LIQUID CRYSTAL DISPLAY DEVICE AND METHOD FOR DRIVING THE SAME — Examiner: S. K. Kumar

APPEAL BRIEF TRANSMITTAL FORM

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is an Appeal Brief on behalf of the Appellants in connection with the above-identified application.

☐ The enclosed document is being transmitted via the Certificate of Mailing provisions of 37 C.F.R. § 1.8.

A Notice of Appeal was filed on April 2, 2007.

☐ Applicant claims small entity status in accordance with 37 C.F.R. § 1.27.

The fee has been calculated as shown below:

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If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: June 4, 2007

Respectfully submitted,

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Attachment: Appeal Brief
Appendix A-C

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APPEAL BRIEF

Commissioner for Patents
P. O. Box 1450
Alexandria, Va. 22313-1450

Sir:

Appellants hereby appeal from the decision in the final Office Action dated November 1, 2006 finally rejecting claims 1, 3-16, 19 and 20.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1205:

I. Real Party In Interest
II Related Appeals and Interferences
III. Status of Claims
IV. Status of Amendments
V. Summary of Claimed Subject Matter
VI. Grounds of Rejection to be Reviewed on Appeal
VII. Argument
VIII. Claims
IX. Evidence
X. Related Proceedings
Appendix A – Claims
Appendix B – Evidence (None)
Appendix C – Related Proceedings (None)

I. REAL PARTY IN INTEREST

The real party in interest for this application is LG Philips LCD Co., Inc. by an Assignment recorded at Reel No. 012420 and Frame 0478. .

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellants' knowledge, there are no other prior or pending appeals of this application, or patent interference proceedings, or judicial proceedings which may be related to, directly affect, or be directly affected by, or have a bearing on the Board's decision of this Appeal.

III. STATUS OF CLAIMS

In the application on appeal, claims 1, 3-16, 19 and 20 are pending. Claims 1 and 11 are independent. Claims 1, 3-16, 19 and 20 are rejected and are on appeal.

IV. STATUS OF AMENDMENTS

The Amendment under 37 CFR 1.116, filed on February 1, 2007, has been entered for purposes of appeal, as noted in the Advisory Action dated March 1, 2007. The status of the claims is correctly stated in that Amendment.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Claim 1 is directed to an LCD device, comprising: a LCD panel (shown as element 41, for example, in Figs. 4 and 6, and described, for example, in paragraphs [0046] and [0048], i.e., from page 10, second last line, through page 11, line 16); a plurality of source drivers applying data signals to the LCD panel (shown, for example, as elements 43 in Figs. 4 and 6, and described, for example, in figs. [0046] and [0048], i.e., from page 10, second last line, through page 11, line 16); a plurality of gate drivers applying gate driving signals to the LCD panel (shown, for example, as element 45, in Figs. 4 and 6, and described, for example, in Figs. [0046] and [0048], i.e., from page 10, second last line, through page 11, line 16); a timing controller (shown as element 47, for example, in Figs. 4 and 6, and described, for example, in Figs. [0046] and [0048], i.e., from page 10, second last line, through page 11, line 16) outputting to the

respective source drivers (43) at least two clock signals having different phases, the timing controller separately outputting R/G/B data synchronized with each clock signal to the source drivers (shown, for example, in Figs. 4 and 6 and described, for example, in paragraphs [0047]-[0051], i.e., from page 11, line 3 through page 12, line 14); and at least two data buses transmitting the data separately output from the timing controller to each of the source drivers, respectively (shown, for example, in Figs. 4 and 6, and described in paragraph [0048], i.e., page 11, lines 11-16), wherein the at least two data buses are connected between the timing controller and each of the source drivers (shown, for example, in Figs. 4 and 6, and described in paragraphs [0047]-[0051], i.e., from page 11, line 3 through page 12, line 14), a number of the data buses are in proportion to a number of clock signals output from the timing controller (shown, for example, in Figs. 4-7 and described in paragraphs [0027], i.e., page 6, lines 12-15, and [0029], i.e., from page 6, line 21 through page 7, line6, and in originally filed claim 3) the source drivers separately sample the data to thereby reduce electricity consumption (as described, for example, in paragraphs [0054], i.e., page 13, lines 6-11, and [0064], i.e., page 16, lines 14-19).

Claim 11 is directed to a method for driving an LCD device having a timing controller transmitting digital data received from a system to each source driver (the device is shown in Figs. 4 and 6 and discussed in paragraphs [0045], i.e., page 10, lines 18-22, and [[0057], i.e., page 13, second last line, through page 14, line2) , comprising the steps of:

providing a timing controller and a plurality of source drivers (disclosed, for example, in paragraphs [0045] , i.e., page 10, lines 18-22, and [0046], i.e., page 10, second late line through page 13, line 2);

outputting from the timing controller at least two clock signals having different phases to each source driver (disclosed, for example, in paragraph [0031], i.e., page 7, line 17, through page 18, line 5); and

separately outputting from the timing controller the digital data to each source driver through both of at least two data buses, the digital data being synchronized with respective clock signals per odd/even numbered data or R/G/B display data (disclosed, for example, in paragraphs [0031]-[0034], i.e., from page 7, line 17, through page 9, line 3),

wherein the at least two data buses are connected between the timing controller and each source driver, respectively, a number of the data buses are in proportion to a number of clock signals output from the timing controller (shown, for example, in Figs. 4 and 6, and described, for example, in paragraphs [0047]-[0051], i.e., from page 11, line 3 through page 12, line 14), and the source drivers separately sample the digital data to thereby reduce electricity consumption (as described, for example, in paragraphs [0054], i.e., page 13, lines 6-11, and [0064], i.e., page 16, lines 14-19).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Initially, Appellant notes that the rejection of claims 1 and 2-10 stand under 35 USC §112, second paragraph, for being indefinite, has been withdrawn per the statement in the continuation sheet attached to the Advisory Action dated March 1, 2007.

1. Claims 1, 5, 11, 16, 19 and 20 stand finally rejected under 35 U.S.C. §102(e)/103(a) as being unpatentable over U.S. patent 6,529,181 to Nakano et al. ("Nakano").

2. Claims 3, 4, 7-9, 12-15, 17 and 18 stand finally rejected under 35 U.S.C. §103(a) as being obvious over Nakano in view of Uchino (U.S. Patent 6,040,816).

3. Claims 2, 6 and 10 stand finally rejected under 35 USC §103(a) as being unpatentable over Nakano in view of U.S. Patent 5,252,957 to Itakura.

VII. ARGUMENT

Claims 1, 5, 11, 16, 19 and 20 stand finally rejected under 35 U.S.C. §102(e)/103(a) as being unpatentable over U.S. Patent 6,529,181 to Nakano et al. ("Nakano"). This rejection is respectfully traversed and should be reversed for reasons set forth, below.

During patent examination the PTO bears the initial burden of presenting a *prima facie* case of unpatentability. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). This burden can be satisfied when the PTO presents evidence, by means of some teaching, suggestion or inference either in the applied prior art or generally available knowledge, that would have appeared to have suggested the claimed subject matter to a person of ordinary skill in the art or would have motivated a person of ordinary skill in the art to combine the applied references in the proposed manner to arrive at the claimed invention. See Carella v. Starlight Archery Pro Line Co., 804 F.2d 135, 140, 231 USPQ 644, 647 (Fed. Cir. 1986); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); In re Rinehart, 531 F.2d 1048, 1051-1052, 189 USPQ 143, 147 (CCPA 1976).

If the PTO fails to meet this burden, then the Appellant is entitled to the patent. However, when a *prima facie* case is made, the burden shifts to the Appellant to come forward with evidence and/or argument supporting patentability. Patentability *vel non* is then determined on the entirety of the record, by a preponderance of evidence and weight of argument, *Id.*

A prior art reference anticipates the subject matter of a claim when that reference discloses every feature of the claimed invention, either explicitly or inherently. In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997) and Hazani v. Int'l Trade Comm'n, 126 F.3d 1473. 1477. 44 USPQ2d 1358, 1361 (Fed Cir. 1997). While, of course, it is possible that it is inherent in the operation of the prior art device that a particular element operates as theorized by the Examiner, inherency may not be established by probabilities or possibilities. In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (CCPA 1981) and In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993).

Because the rejection is based on 35 U.S.C. §103, what is in issue in such a rejection is "the invention as a whole," not just a few features of the claimed invention. Under 35 U.S.C. §103, " [a] patent may not be obtained . . . if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." The determination under §103 is whether the claimed invention as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made. See In re O'Farrell, 853 F.2d 894, 902, 7 USPQ2d 1673, 1680 (Fed. Cir. 1988). In determining obviousness, the invention must be considered as a whole and the claims must be

considered in their entirety. See Medtronic, Inc. v. Cardiac Pacemakers, Inc., 721 F.2d 1563, 1567, 220 USPQ 97, 101 (Fed. Cir. 1983).

In rejecting claims under 35 U.S.C. §103, it is incumbent on the Examiner to establish a factual basis to support the legal conclusion of obviousness. See, In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one of ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal Inc. v. F-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the Examiner are an essential part of complying with the burden of presenting a *prima facie* case of obviousness. Note, In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992). To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be suggested or taught by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1970). All words in a claim must be considered in judging the

patentability of that claim against the prior art. In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

A showing of a suggestion, teaching, or motivation to combine the prior art references is an "essential evidentiary component of an obviousness holding." C.R. Bard, Inc. v. M3 Sys. Inc., 157 F.3d 1340, 1352, 48 USPQ2d 1225, 1232 (Fed. Cir. 1998). This showing must be clear and particular, and broad conclusory statements about the teaching of multiple references, standing alone, are not "evidence." See In re Dembiczak, 175 F.3d 994 at 1000, 50 USPQ2d 1614 at 1617 (Fed. Cir. 1999).

Moreover, it is well settled that the Office must provide objective evidence of the basis used in a prior art rejection. A factual inquiry whether to modify a reference must be based on objective evidence of record, not merely conclusory statements of the Examiner. See, In re Lee, 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).

Furthermore, during patent examination, the PTO bears the initial burden of presenting a *prima facie* case of unpatentability. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). If the PTO fails to meet this burden, then the Appellant is entitled to the patent. Only when a *prima facie* case is made, the burden shifts to the Appellant to come forward to rebut such a case.

Initially, it is not clear what the actual statutory basis for this rejection is. On page 2 of the final Office Action, the section heading above paragraph No. 3 states "Claim Rejections – 35 USC §102", whereas, the rejection in paragraph 5 on page 3 states that the rejection is under 35 USC §103(a). Clarification was respectfully requested in the Amendment filed on March 1, 2007, but this issue does not appear to have been addressed in the Advisory Action.

Regardless of the statutory basis for the rejection, Appellant respectfully submits that Nakano fails to either anticipate, or render obvious, the claimed invention should be reversed for a number of reasons.

Firstly, the claimed invention recites a combination of features, including "a plurality of source drivers." Nakano clearly does not disclose or suggest "source drivers." The Office Action incorrectly indicates that elements 130 in Nakano are source drivers. Actually, elements 130 in Nakano are disclosed as "drain drivers" throughout Nakano's specification. See, in this regard, col. 4, lines 48-55 of Nakano.

Secondly, Nakano does not provide at least two clock signals to each source driver (130 or 130' or 130"), as recited. For example, as explained in col. 6 of Nakano, starting in line 30, a single clock signal D4 is transmitted to a group A of odd numbered drain drivers 130 in Fig. 1 through a signal line 131, whereas a different single clock signal D5 in turn is transmitted to a group B of even-numbered drain drivers 130 in Fig. 1 through a signal line 132. In other words, each odd numbered drain driver 130 and each even numbered drain driver 130 are provided with just a single clock signal. This differs from what is positively recited in claims 1 and 11, each of which positively recites a timing controller outputting to each of the source drivers at least two clock signals.

Thirdly, Nakano does not provide at least two data buses connected between the timing controller and each of the source drivers, as positively recited in claims 1 and 11. For example, as shown in Figs. 5A and 15A of Nakano, only a single bus line is connected to each drain driver. Similarly, only one data bus line 134 is shown in Fig. 1 of Nakano as being connected to a single drain driver 130. While Nakano actually discloses using two bus lines 134a and 134b in

Figs. 5A and 5B, Nakano discloses connecting them alternatively to the drain drivers 130, instead of connecting both buses to a single drain driver.

Accordingly, Nakano neither anticipates nor suggests, nor otherwise renders obvious, the claimed invention of independent claims 1 and 11, or of dependent claims 5, 16, 19 and 20, each of which depends from one of those independent claims.

Concerning the language "and the source drivers separately sample the data to thereby reduce electricity consumption," Appellant respectfully submits that Nakano does not achieve this claimed feature, because it does not disclose or suggest that at least two data buses are connected between the timing controller and each of the source drivers to achieve this. The argument that the claimed structure is taught by Nakano is incorrect, for reasons pointed out above. The Office Action fails to achieve this claimed feature because Nakano does not disclose or suggest the claimed structure or the same function. Moreover, as pointed out above, to make out a *prima facie* case of inherency, the Office must provide objective factual evidence that what is alleged to inherently occur, must occur not just possibly, or not just probably, but must necessarily occur. Such a showing has not been made in this rejection. Furthermore, because Nakano dies not disclose at least two clock signals to each source driver, as recited, Nakano does not have the same structure as claimed, so the argument that the same structure will function in the same way, does not apply to this claimed invention. The argument also does not apply because just because two devices may have the same structure does not mean that the electronic signals transmitted through that structure are the same. If this argument were correct, then circa 1950's telephone exchange signals would inherently operate the same way as a circa 2007 DSL network over the same telephone lines.

Claim 1 positively recites a combination of features, including a timing controller outputting to the respective source drivers at least two clock signals having different phases, the timing controller separately outputting R/G/B data synchronized with each clock signal to the source drivers; and at least two data buses transmitting the data separately output from the timing controller to each of the source drivers, respectively (emphasis added).

This claimed combination of features is neither disclosed nor suggested by Nakano for a number of reasons.

Firstly, data transmitting sequence of the present invention is different from that of Nakano. Nakano discloses that data (1, 2, 3...)(1, n+1...) for odd drain drivers are provided to the odd drain drivers through the bus A, and data (n+1, n+2, n+3...)(2n+1, 3n+1...) for even drain drivers are provided to the even drain drivers through the bus B. (shown, for example, in Fig. 5B and 15B, and described)

FIG. 5B

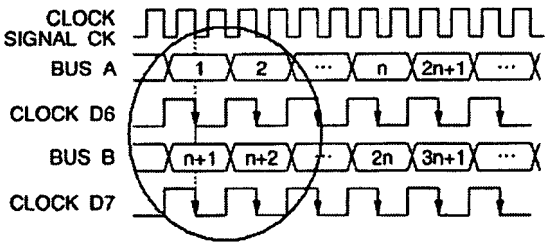
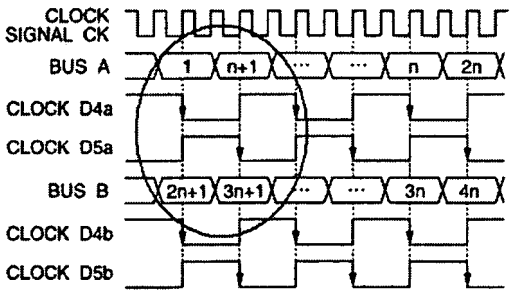


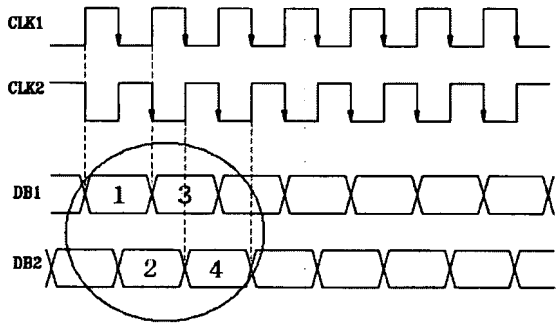
FIG. 15B



On the other hand, the present invention discloses that data (1, 3, 5...) for odd pixel are provided to the respective source drivers through the first data bus DB1, and data (2, 4, 6...) for even pixel are provided to the respective source drivers through the second data bus DB2. That is, the present invention discloses that data providing respective source drivers are provided

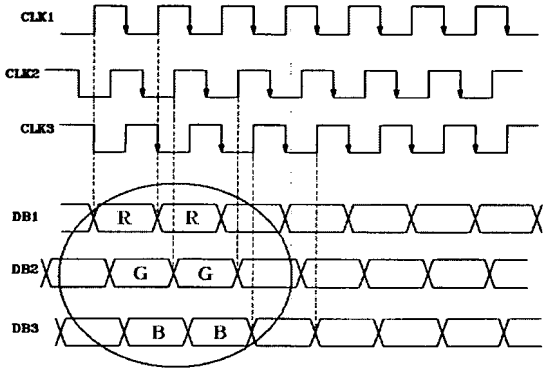
alternately to the first and second data buses DB1 and DB2. (shown, for example, in Fig. 5, and described, for example, in paragraphs [0050]-[0051])

FIG. 5



Secondly, the present invention discloses that red data(R) for red pixel are provided to the respective source drivers through the first data bus DB1, green data(G) for green pixel are provided to the respective source drivers through the second data bus DB2, and blue data(B) for blue pixel are provided to the respective source drivers through the third data bus DB3. (shown, for example, in Fig. 7, and described)

FIG. 7



Thirdly, Phase of data synchronized with each clocks of the present invention is different from that of the Nakano. Nakano discloses that data transmitted to bus A and bus B have same phases (shown, for example, in Fig. 5B and 15B, and described).

On the other hand, the present invention discloses that data output from timing controller to data buses DB1 and DB2 have different phases such that the phases of data are synchronized with each clock.

Thus, Nakano fails to teach or suggest the feature of present invention as "a timing controller outputting to the respective source drivers at least two clock signals having different phases, the timing controller separately outputting R/G/B data synchronized with each clock signal to the source drivers" and/or "at least two data buses transmitting the data separately output from the timing controller to each of the source drivers, respectively".

Accordingly, reconsideration and reversal of this rejection of claims 1, 5, 11, 16, 19 and 20, under whatever statutory basis it is made, are respectfully requested.

Claims 3, 4, 7-9, 12-15, 17 and 18 stand finally rejected under 35 U.S.C. §103(a) as being obvious over Nakano in view of Uchino (U.S. Patent 6,040,816). This rejection is respectfully traversed and should be reversed for at least the following reasons.

Initially, Appellant respectfully notes that Nakano does not disclose or render obvious the invention recited in independent claims 1 and 11, and that Uchino is not applied to remedy the aforenoted deficiencies in Nakano. Thus, even if one of ordinary skill in the art were properly motivated to modify Nakano in view of Uchino, as suggested, the resulting modified version of Nakano would not disclose, or suggest, or otherwise render obvious, the claimed invention.

Moreover, the Office Action fails to present objective factual evidence of proper motivation for one of ordinary skill in the art to modify Nakano, as suggested, in view of Uchino. Appellant respectfully submits that Nakano and Uchino differ from one another in a manner

which teaches away from the proposed combination of these two references. In this regard, Appellant notes that these two devices of Nakano & Uchino differ in their fundamental mode of operation in that Nakano supplies its data pulses to the drain electrodes of its transistors, whereas Uchino supplies its data pulses to the source electrodes of its transistors, Uchino's drain electrodes being connected to its pixel electrodes. Accordingly, Appellant respectfully submits that the modification of Nakano in view of Uchino would result in an inoperative device.

A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the Appellant. The degree of teaching away will of course depend on the particular facts; in general, a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the Appellant. See W.L. Gore & Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1550-51, 220 USPQ 303, 311 (Fed. Cir. 1983) (the totality of a reference's teachings must be considered), cert. denied, 469 U.S. 851 (1984); In re Sponnoble, 405 F.2d 578, 587, 160 USPQ 237, 244 (CCPA 1969) (references taken in combination teach away since they would produce a "seemingly inoperative device"); In re Caldwell, 319 F.2d 254, 256, 138 USPQ 243, 245 (CCPA 1963) (reference teaches away if it leaves the impression that the product would not have the property sought by the Appellant). See, In re Gurley, 31 USPQ2d 1130 (Fed. Cir. 1994).

The Office Action then relies on Fig. 2 of Uchino, which shows a timing chart for an active matrix LCD device which has a problem of dispersion of phase among sampling pulses which Uchino is designed to correct. In other words, the embodiment of Uchino on which this

rejection is based is an embodiment that Uchino tries to correct, by referring to a conventional phase dispersion solution embodiment (Fig. 4) and by referring to a phase dispersion solution embodiment of its own (Figs. 6-10). Appellant respectfully submits that one of ordinary skill in the art would definitely not be motivated to modify Nakano using a scheme that is eschewed by Uchino in the sense that the timing scheme of Uchino relied on in this rejection is taught by Uchino to create the phase dispersion problem that its invention solves. In other words, Uchino teaches away from modifying Nakano as suggested because the source of the suggestion is in an embodiment of Uchino which has the problem that Uchino is directed to solve, and the timing associated with Uchino's dispersion solution does not have that timing feature.

In the Advisory Action continuation sheet, the Examiner argues that the basis for proper motivation to modify Nakano in view of Uchino is "in order to reduce the amount of crosstalk and thereby enhancing the resolution of the LCD panel." Appellant respectfully disagrees with this conclusion not only because of the previously presented reasons why these references teach away from being combined, as suggested, but also because Nakano does not demonstrate that it has a crosstalk problem that needs to be addressed, and explicitly discloses that its lower frequency clock signals are used to overcome difficulties with higher resolution displays (col. 2, lines 55-64), thus achieving improved resolution LCD devices, thereby not demonstrating a need to address suppression of phase dispersion of sampling pulses, to which Uchino is directed (col. 3, lines 40-43).

Accordingly, not only does the final Office Action fails to make out a *prima facie* case of proper motivation to modify Nakano as suggested, but even if proper motivation existed, the resulting modification of Nakano would not result in, suggest, or otherwise render obvious, the

claimed invention because Nakano does not disclose or render obvious the invention recited in independent claims 1 and 11, and Uchino is not applied to remedy the aforenoted deficiencies in Nakano.

Thus, the final rejection fails to make out a *prima facie* case of obviousness of the claimed invention.

Reconsideration and reversal of this rejection of claims 3, 4, 7-9, 12-15, 17 and 18 are respectfully requested.

Claims 2, 6 and 10 stand rejected under 35 USC §103(a) as being unpatentable over Nakano in view of U.S. Patent 5,252,957 to Itakura. This rejection is respectfully traversed.

Initially, Appellant notes that claim 2 was canceled in the Amendment filed on August 4, 2006, so this rejection is moot with respect to claim 2.

Furthermore, Appellant respectfully notes that Nakano does not disclose or render obvious the invention recited in independent claims 1 and 11, and that Itakura is not applied to remedy the aforenoted deficiencies in Nakano. Thus, even if one of ordinary skill in the art were properly motivated to modify Nakano in view of Itakura, as suggested, the resulting modified version of Nakano would not disclose, or suggest, or otherwise render obvious, the claimed invention.

Accordingly, the final Office Action fails to make out a *prima facie* case of obviousness of the claimed invention.

Reconsideration and reversal of this rejection of claims 2, 6 and 10 are respectfully requested.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

IX. EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the Examiner is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in Section II, above.

CONCLUSION

For the reasons presented above, Appellants respectfully submit that the outstanding rejections of record should be revered and this Application returned to the Examiner for allowance.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: June 4, 2007

Respectfully submitted,

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APPENDIX A - Claims

1. (Previously Presented) An LCD device, comprising:

a LCD panel;

a plurality of source drivers applying data signals to the LCD panel;

a plurality of gate drivers applying gate driving signals to the LCD panel;

a timing controller outputting to the respective source drivers at least two clock signals having different phases, the timing controller separately outputting R/G/B data synchronized with each clock signal to the source drivers; and

at least two data buses transmitting the data separately output from the timing controller to each of the source drivers,

wherein the at least two data buses are connected between the timing controller and each of the source drivers, a number of the data buses are in proportion to a number of clock signals output from the timing controller, and the source drivers separately sample the data to thereby reduce electricity consumption.

2. (Cancelled)

3. (Previously Presented) The LCD device as claimed in claim 1, wherein the timing controller outputs the data synchronized with a rising edge time of each clock signal.

4. (Previously Presented) The LCD device as claimed in claim 1, wherein the timing

controller outputs the data synchronized with a falling edge time of each clock signal.

5. (Original) The LCD device as claimed in claim 1, wherein the timing controller outputs first and second clock signals having opposite phases to each other.

6. (Original) The LCD device as claimed in claim 1, wherein the timing controller outputs first, second and third clock signals, each having different phases to each another.

7. (Original) The LCD device as claimed in claim 4, wherein the source driver samples data in the falling edge time when the data synchronized with the rising edge time is output.

8. (Original) The LCD device as claimed in claim 5, wherein the source driver samples data in the rising edge time when the data synchronized in the falling edge timing is output.

9. (Previously Presented) The LCD device as claimed in claim 5, wherein odd numbered display data is output synchronized with a rising edge of the first clock signal, and even numbered display data synchronized with a rising edge of the second clock signal is output.

10. (Previously Presented) The LCD device as claimed in claim 6, wherein data for displaying R color is output synchronized with a rising edge of the first clock signal, data for displaying G color is output synchronized with a rising edge of the second clock signal, and data for displaying B color is output synchronized with a rising edge of the third clock signal.

11. (Previously Presented) A method for driving an LCD device having a timing controller transmitting digital data received from a system to each source driver, comprising the steps of:

providing a timing controller and a plurality of source drivers;

outputting from the timing controller at least two clock signals having different phases to each source driver; and

separately outputting from the timing controller the digital data to each source driver through both of at least two data buses, the digital data being synchronized with respective clock signals per odd/even numbered data or R/G/B display data,

wherein the at least two data buses are connected between the timing controller and each source driver, respectively, a number of the data buses are in proportion to a number of clock signals output from the timing controller, and the source drivers separately sample the digital data to thereby reduce electricity consumption

12. (Previously Presented) The method as claimed in claim 11, wherein the digital data is synchronized with a rising edge of each clock signal.

13. (Previously Presented) The method as claimed in claim 12, wherein each source driver samples the digital data synchronized with a falling edge of each clock signal if the digital data is output synchronized with the rising edge of each clock signal.

14. (Previously Presented) The method as claimed in claim 11, wherein the digital data is output synchronized with a falling edge of each clock signal.

15. (Previously Presented) The method as claimed in claim 14, wherein each source driver samples the digital data synchronized with a rising edge of each clock signal if the digital data is output synchronized with the falling edge of each clock signal.

16. (Previously Presented) The method as claimed in claim 11, wherein two clock signals having different phases are used when the digital data is separately output according to odd and even numbered data, and three clock signals having different phases are used when the data is separately output according to R/G/B data.

17-18. (Cancelled)

19. (Previously Presented) The LCD device as claimed in claim 1, wherein the at least two data buses are separated from each other.

20. (Previously Presented) The method as claimed in claim 11, wherein the at least two data buses are separated from each other.

APPENDIX B – EVIDENCE

(None)

APPENDIX C – RELATED PROCEEDINGS

(None)